Circuit Design and Verification of 7nm Low-Power, Low-Jitter PLLs for HSC, Automotive, and IoT

Silicon Creations / Mentor, a Siemens Business

ABSTRACT

The connectivity required for consumer, data center, automotive, and Internet of Things (IoT) applications places stringent specification requirements on one of the most critical components, the Phase-Locked Loop (PLL). PLLs demodulate wireless signals, enable high-speed SerDes channels, synthesize stable frequencies with high resolution, or distribute precisely timed clocks in digital circuits.

Silicon Creations supplies high-performance semi-custom analog and mixed-signal IP including PLLs, free-running oscillators, high-speed I/O, and SerDes. Silicon Creations uses Mentor's Calibre Platform for IC verification and sign-off and Analog FastSPICE Platform (AFS) for nanometer circuit verification and sign-off. With AFS, designers are able to perform large analog circuit simulation and noise analysis with nanometer SPICE accuracy while increasing their productivity. AFS is certified in the TSMC SPICE-Qualification Program, including 7nm FF nodes, and AFS Full-Spectrum device noise analysis is part of the TSMC Custom Design Reference Flow.

In this paper, we will describe the challenges associated with achieving silicon-accurate design and verification of several different PLLs and oscillators fabricated in the TSMC 7nm FF processe. We will provide details on the verification of several IPs including a low jitter fractional PLL with 24-bit resolution, an IoT PLL with <15µW, 32 kHz, an area optimized digital clocking PLL (0.009mm2), and a low power (<30µW) free-running oscillator with <1.5% frequency variation across temperature and supply voltage. We will also show results of AFS Periodic Noise analysis and AFS Transient Noise analysis with great correlation to silicon measurement (1-2dB) and excellent simulation run time. In addition, AFS is used for aging and EOS (electrical overstress) simulation on all IP.

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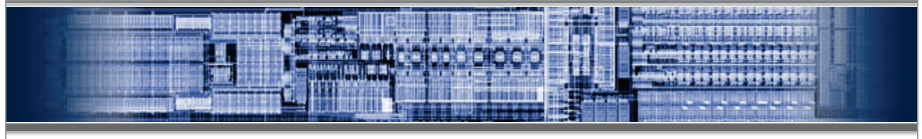

Circuit Design and Verification of 7nm Low-Power, Low-Jitter PLLs for HSC, Automotive, and IoT

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Introduction

- Presenting verification results of 7nm Low-Power, Low-Jitter PLLs
- Three way collaboration between:
  - Silicon Creations: 7nm precision analog IP development
  - TSMC: 7nm process with silicon accurate models
  - Mentor: Analog FastSPICE™ Platform

Silicon Creations

tsmc Open Innovation Platform®

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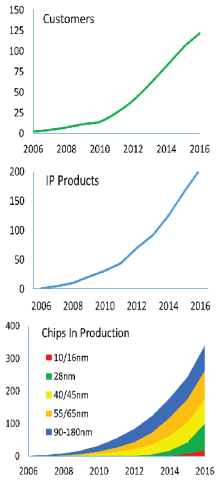
Overview

- Silicon Creations achieved first-pass silicon success in TSMC 7nm
  - Multiple PLLs and oscillators are meeting predicted performance specs
  - Volume production is expected soon
- Advanced Mentor tool flow to develop 7nm IP
  - Analog FastSPICE Platform for accurate performance analysis including transient and Full-Spectrum Device Noise
  - Calibre DRC/LVS/XACT-3D/PERC for reliable back-end verification
- Reliable SPICE models and process consistency from TSMC
  - Measured results show minimal process variation and Gaussian spread

Outline

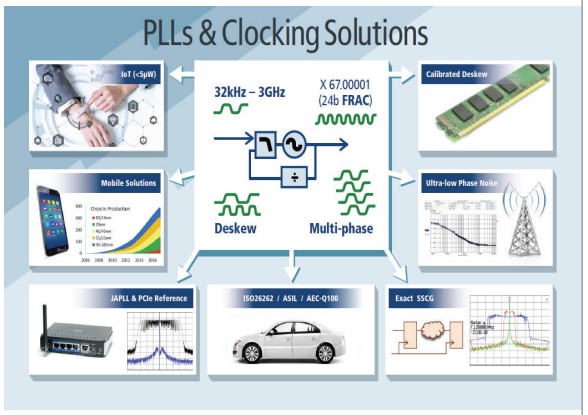
Introduction

- Since 2006, Silicon Creations has provided over 200 analog/mixed-signal IP designs, from TSMC 350nm down to 7nm
  - 170 different PLL designs
  - 9 designs (PLLs and Oscillators) in TSMC 7FF
  - 300+ customer chips with this IP in production at TSMC
- Silicon Creations target segments
  - Consumer
  - Data Center
  - IoT
  - Automotive
  - Aerospace
  - Industrial



Silicon Creations Products - PLLs

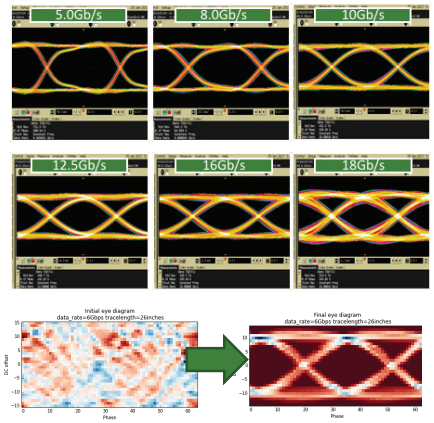
- PLLs are some of the highest volume analog IPs
  - Example PLLTS28HPMFRAC is on 93 different production chips, 600k+ wafers, >1B instances in production
  - Requires robust design, good QA!
- PLL products include general purpose, low jitter (AFE/SERDES), mW IoT, Automotive



Silicon Creations Products – SERDES

Robust architecture, well proven, low risk, low power

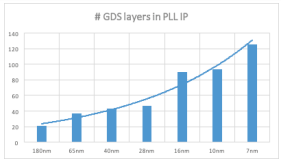
- Production from 28nm to 180nm and from <100Mbps to 20Gbps
- Our SERDES have a wide tuning range (up to 16:1) with random jitter less than 0.5ps RMS
- Standards including PCIe, 10GKR, XAUI, SATA, V-by-1 HS, FastLVDS, CameraLink, FPDLink, RapidIO, OIF-CEI, JESD204, CPRI and semi-custom links
- Examples shown from 12.7Gb/s multiprotocol with DFE, Eye Monitor

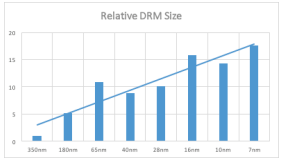


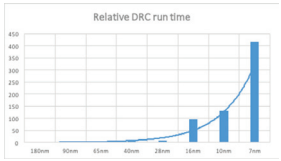
Outline

7nm Design Challenges - Process Complexity

- Number of GDS layers
  - A simple measure of process complexity PLL IP
  - The number of layers has increased 5x since 180nm
- Relative DRM size
  - From .35mm to FinFET, the DRM thickness has increased over an order of magnitude
  - Does the ~15x increase in DRM thickness indicate the process complexity?
- Relative DRC Run Time
  - Tighter more complex rules
  - More fill geometries
  - 16nm FinFET run times are ~10x the 28nm run times
  - 7nm FinFET run times are ~50x!
- Quite complex! Quite expensive!

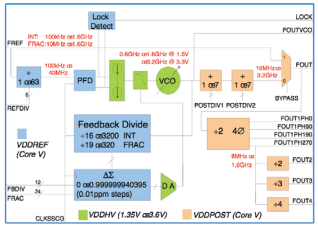


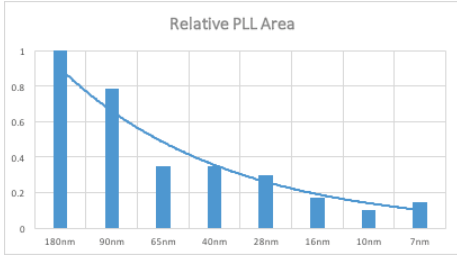




7nm Design Challenges - Analog Scaling

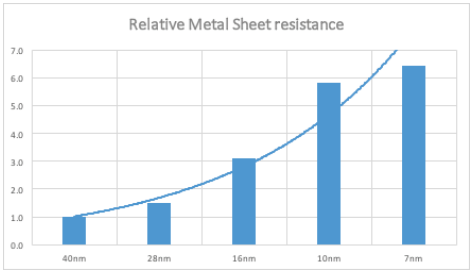
- There is some debate over whether analog "scales"
- The plot on the right shows the area for Silicon Creations' PLLs with similar frequency & jitter specs from 180nm to 7nm
- Holding noise constant (kT/C), the area should scale with cap area – and does!
- So, analog functions scale, but not as well as digital functions
  - Digital scaling from 180nm to 7nm is ~661:1
  - Analog scaling from 180nm to 7nm is ~10:1





7nm Design Challenges - Interconnect

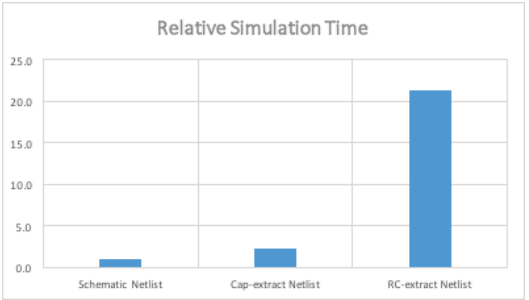
- The role of extraction and post extract simulations is becoming more important
- Interconnect resistance is climbing quickly!
- From 40nm to 7nm, the relative wire resistance (Ohms/sq) has risen more than 6 fold



- The impact of resistance is leading to multiple challenges:
  - Designs are becoming limited more and more by wire performance
  - Designs are increasingly difficult to verify due to the need for simulation of distributed RC parasitics

7nm Design Challenges - Simulation Time

- In advanced processes, the interconnect resistance must be taken into account
- Schematic sims are out, CC and RC extracted sims are needed!
- This simulation time translates to:
  - Longer development cycles
  - Need for more simulation licenses
  - Need for parallel simulation licenses
  - Higher development costs!
- Simulation of interconnect + devices is expensive!



Note: RC reduction can help reduce simulation times!

Outline

Custom IP Verification Challenges

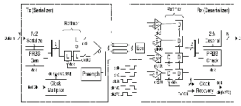
- Traditional SPICE simulators do not have performance and capacity
- Need nanometer SPICE accuracy to validate key specifications
- Need tighter tolerances to increase the dynamic range (>100dB)
- Need to include layout parasitics and device noise
- Long runs for verification and characterization

Fractional-N LC PLL		Specification
Critical Specs	Lock Range	1.6GHz to 3.2GHz
	Output Jitter	0.26ps RMS
	Phase noise @ 1MHz	-125dBc/Hz
	Reference spur	-71dBc
	Loop bandwidth	30kHz
	Power consumption	53mW @ 3.2GHz

- Accuracy
  - –60-120 dB dynamic range
  - –Device noise bandwidth
- Long runs
  - –PLL locking, Jitter/phase noise
  - –Integration w/ driven circuitry
- nm circuit characterization
  - –Extracted parasitics: >200k
  - –Device mismatch: >200 iters
  - –PVT corners, process variation

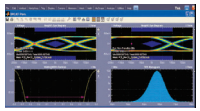
Challenges to Matching Silicon

Simulated Circuit



Uncertainty

Measured Silicon



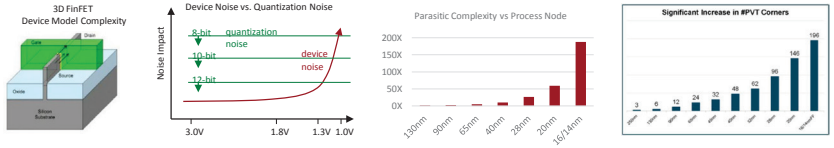
Simulation Uncertainty

- Model accuracy (SPICE, variation, corners)
- Process variation (global & local)
- Parasitic devices (extraction, variation)
- Layout effects
- Thermal effects
- Device noise, noise bandwidth, runtime
- Circuit simulator accuracy (noise floor)
- Distribution uncertainty (sample size)
- Measurement post-processing

Measurement Uncertainty

- Specific silicon manufacturing
- Lot, wafer, and die selection
- Specific contextual circuit activity
- Test equipment (method and resolution)
- Probe effects & variability
- Temperature & variation
- Voltage & variation
- Distribution uncertainty (sample size)
- Measurement post-processing

First Order Nanometer Physical Effects



- Technology Perspective:
  - Need to include device noise effects
  - Need to include huge number of parasitics
  - Need to include impact of lossy channels
  - Increasing device model complexity for FinFET
  - Complex layout effects impacting design specs
- Design Perspective:
  - Reinventing designs for low-supply-voltages
  - Low power applications for analog IP
  - Fully SPICE accurate simulation with very low noise floor
  - Need Monte Carlo and many corners to ensure operation

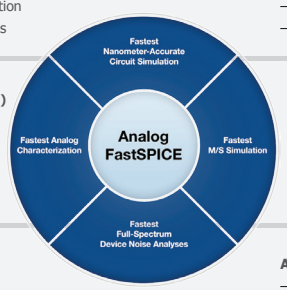
- ➢ Huge Netlists
- ➢ Longer Simulations
- ➢ Lots of Simulations
- ➢ Device Noise Required

Outline

AFS Platform: Quick Overview

AFS Mega
- Embedded SRAM Characterization
- Compatible w/ digital FastSPICE flows
- Accurate power and timing characterization
- Same performance as less accurate tools

AFS Circuit Simulation
- Foundry certified down to 7nm
- 5x-10x faster vs golden SPICE (1-core)
- 2x-6x faster vs parallel SPICE simulators
- >20M-element capacity



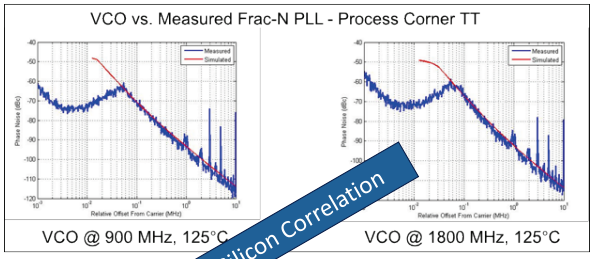
Analog Characterization Environment (ACE)
- High-productivity characterization
- Corner, sweep, and Monte Carlo
- Complex nesting support
- Visual distribution analyzer

AFS AMS
- Easy mixed-signal sim setup
- Runs Verilog and SPICE netlists
- Supports standard Verilog tools
- Leverages AFS differentiation

AFS RF Analyses
- Full-Spectrum periodic noise analysis
- PSS, pnoise, oscnoise, sampled pnoise
- There is no maxsideband parameter
- >100K element PSS convergence

AFS Transient Noise
- Signoff Accuracy for nm designs
- Must have for PLL, ADC/DAC, High-Speed I/O
- Silicon accuracy for Jitter, Phase Noise, SNDR
- Proven to be within 1–2 dB of silicon

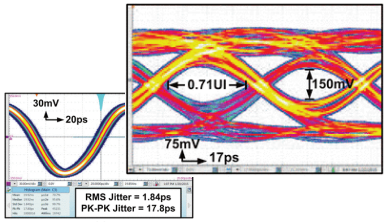
Solving the Verification Challenge with AFS



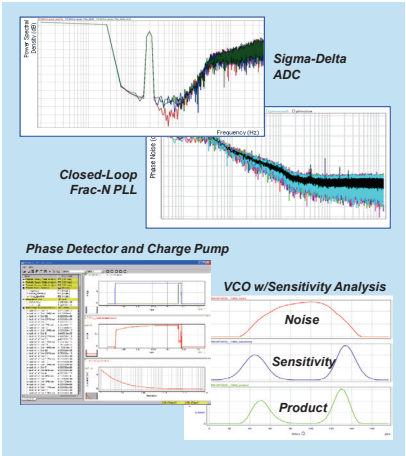
✓ Silicon Correlation

SerDes PLL

Phase Noise (dBc/Hz)	AFS	Silicon	Difference
PLL Setting 1	-114.8	-114.0	0.8
PLL Setting 2	-114.3	-114.0	0.3
PLL Setting 3	-108.8	-108.0	0.8



AFS Full-Spectrum Device Noise Analysis



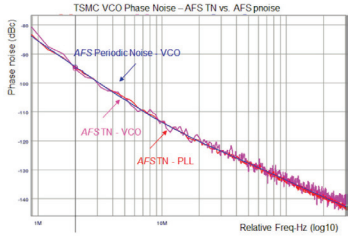
- AFS Full-Spectrum Transient Noise Analysis
  - Transient noise within 1-2dB silicon data
  - Only practical solution for ADCs and PLLs
  - Within 2x AFS runtime (per timestep)
- AFS Full-Spectrum Periodic Noise Analysis
  - Includes all device noise sidebands/harmonics
  - >100K element PSS convergence
  - 5x-10x faster when >100 sidebands
- AFS Full-Spectrum Oscillator Noise Analysis
  - Includes phase and amplitude noise
  - Contribution for every noise source
  - Impulse sensitivity function for every node

TSMC Custom Design Reference Flow

AFS Platform Full-Spectrum Device Noise Analysis

Open Innovation Platform®

AFS Transient Noise Matches AFS pnoise for TSMC PLL



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Problem: Device noise in analog, mixed-signal, and RF circuits limits performance at 45nm and below
Solution: Use device noise analysis to characterize performance of analog, mixed-signal, and RF circuits
Technology: AFS Platform Full-Spectrum Device Noise Analysis for transient noise and periodic noise
Benefit: Verify PLLs, ADCs, SerDes, & others with nm SPICE accuracy including all device noise effects

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Outline

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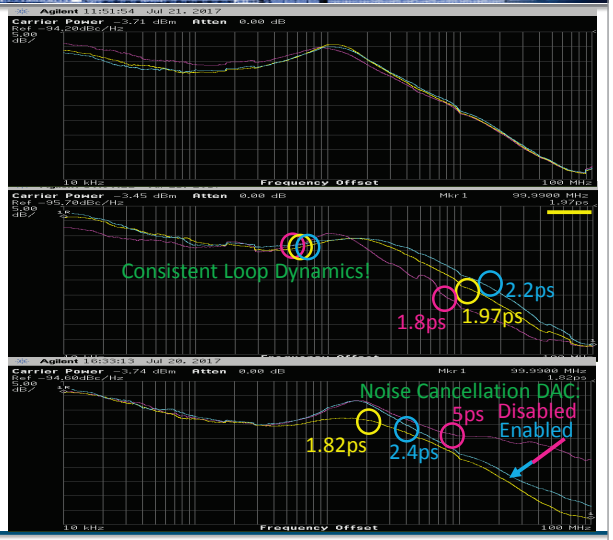
Fractional PLL Phase Noise

- Phase Noise vs. Process Corner
  - FastN/FastP
  - TypN/TypP
  - SlowN/SlowP
- Phase Noise vs. Temperature
  - 125C
  - 27C
  - -40C
- Phase Noise vs. Operating Mode
  - Fractional Mode, Noise cancellation DISABLED
  - Fractional Mode with Noise Cancellation
  - Integer Mode



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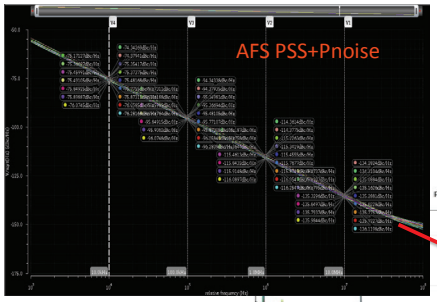
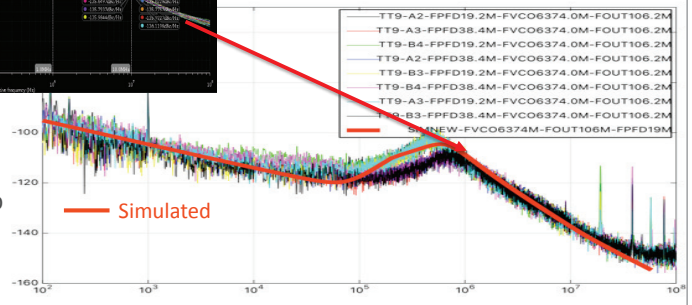
Fractional PLL Simulation vs. Measurement



- Excellent correspondence between AFS derived phase noise and measured performance

- PSS+Pnoise
  - VCO
  - Charge Pump



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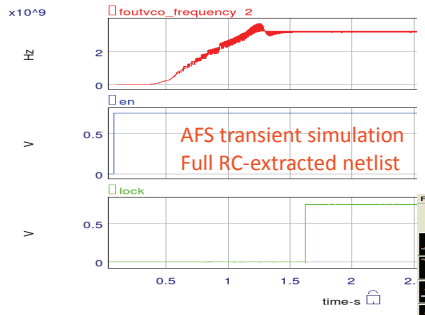
Core Voltage, Area Optimized PLL Locking
Simulation vs. Measurement

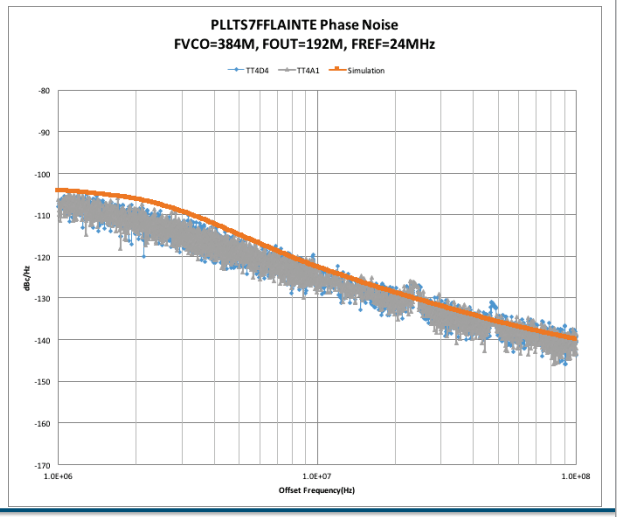


- Excellent correspondence between AFS transient simulation (frequency vs. time) and measured result

- Lowest area PLL for digital clocking
  - 0.009mm^2
- Total power under 200µW

Ultra-Low Power (<100µW), Fast Locking PLL
Phase Noise Correlation

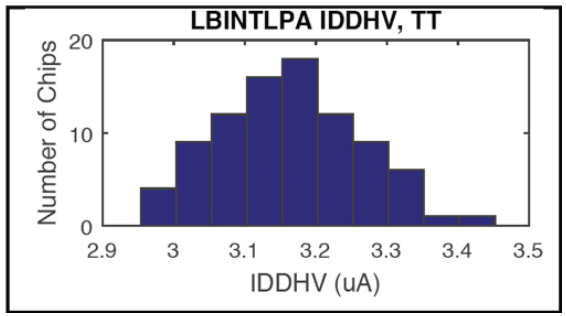
- Phase noise correlation achieved for multiple classes of PLL
- PLL power class covers 3 orders of magnitude
  - ~3µA to ~3mA



IoT PLL Current Consumption

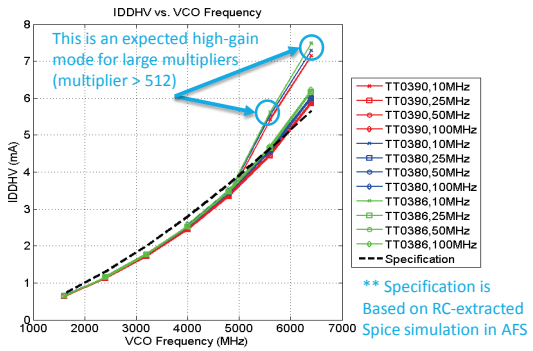
- **Simulation**
  - Mean=3.02uA
  - Stddev=1.5%
- **Measurement**
  - Mean=3.15uA
  - Stddev=1.6%

Measured Current Distribution



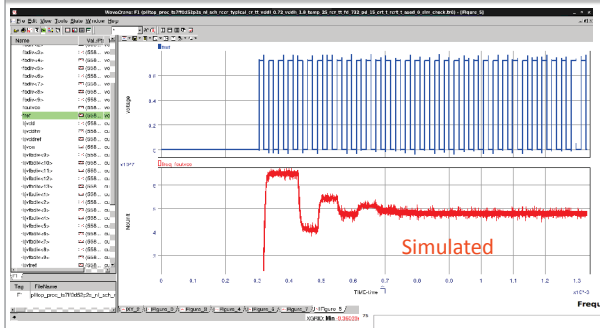
FRAC PLL Current Consumption

- Measured results match simulation across entire VCO range
- Minimal chip-to-chip variation

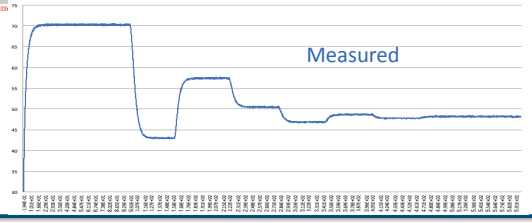


** Specification is Based on RC-extracted Spice simulation in AFS

IoT PLL Fast Locking

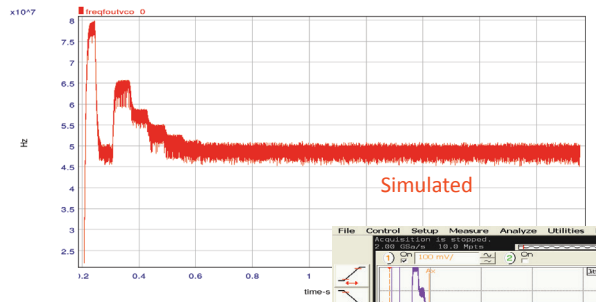


- AFS transient simulations accurately predict locking behavior



- 32kHz locking simulations must run for >1ms, so require fast simulator AND fast locking PLL!

IoT PLL Fast Locking



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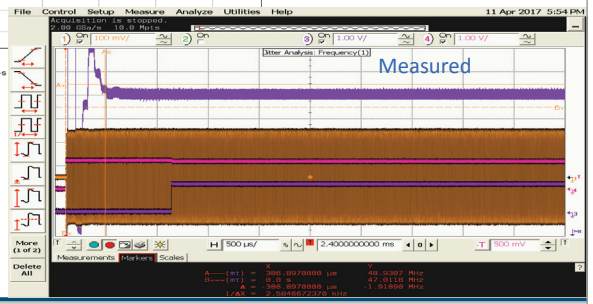
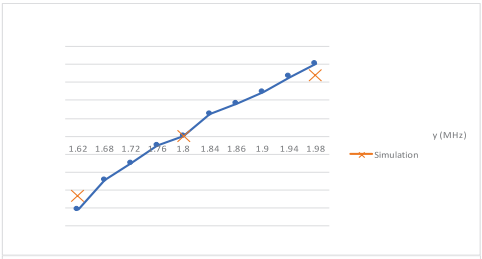
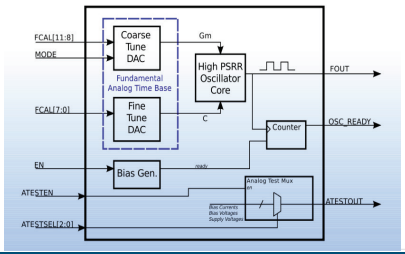


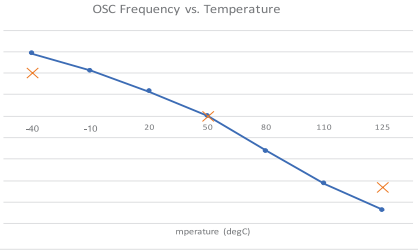
- 32kHz locking simulations must run for >1ms, so require fast simulator AND fast locking PLL!

Oscillator Frequency Stability

- Free-running oscillator provides accurate frequency (without a crystal reference) across all voltage and temperature variations



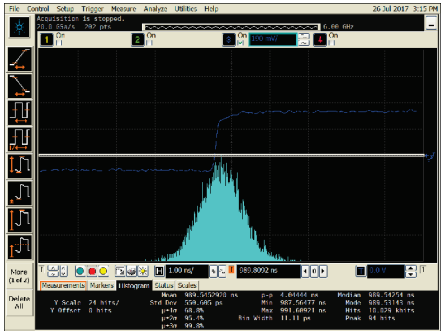




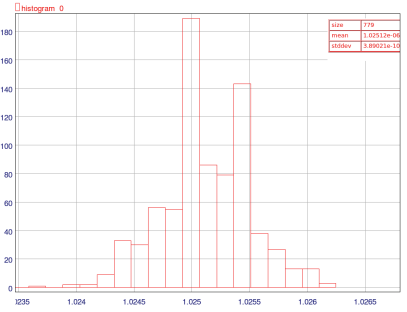
Transient Noise Correlation

- Highly non-linear, ultra-low power (<100µW), free-running oscillator is accurately modeled with AFS Transient Noise analysis

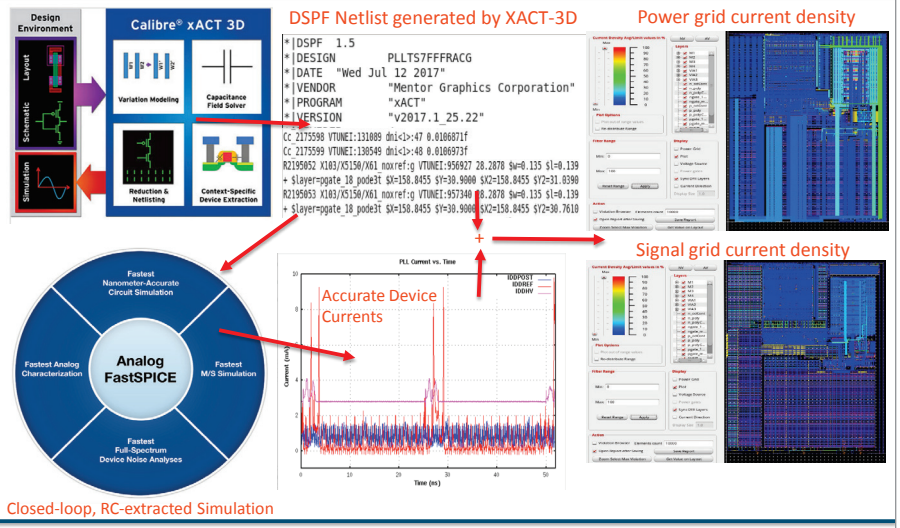
Measured OSCTS7FFRLXB: 0.55ns RMS



Simulated OSCTS7FFRLXB AFS Trannoise Analysis: 0.39ns RMS



EM/IR/EOS Flow



Outline

Summary

- High performance analog and mixed-signal IP (PLLs and Oscillators) has successfully been developed in TSMC 7nm process using Mentor tool flow
- Significant speed improvements from analysis tools allow the 7nm verification to continue to scale, despite increased process complexity
- Mentor's AFS Platform delivered:
  - Excellent correspondence between AFS phase noise and measured performance
  - Phase noise correlation achieved for multiple classes of PLL
  - Measurements match simulation across VCO range with minimal chip-to-chip variation
  - AFS transient simulations accurately predict locking behavior
  - AFS Transient Noise analysis accurately models highly non-linear, ultra-low power (<100µW), free-running oscillator
- TSMC Models predict measured behavior with good confidence